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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Sanduleanu *et al.*	Examiner:	Kinkead, A.
Serial No.:	10/527,946	Group Art Unit:	2817
Filed:	March 15, 2005	Docket No.:	NL 020846 US
Title:	VOLTAGE CONTROLLED LC TANK OSCILLATOR		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being transmitted via facsimile-Formal Entry, to the attention of the Examiner at Commissioner for Patents, MAIL STOP APPEAL BRIEF, P.O. Box 1450, Alexandria, VA 22313-1450, on February 28, 2007.

By: Kelly J. Ledin

Facsimile No.: 571 273-8300

APPEAL BRIEF

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Commissioner For Patents
P.O. Box 1450
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Customer No.
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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed December 29, 2006 and in response to the rejections of claims 1-15 as set forth in the Final Office Action dated October 2, 2006, and in further response to the Advisory Action dated December 18, 2006.

Please charge Deposit Account number 50-0996 (NXPS.215PA) $500.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

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I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 016973/0393 to Koninklijke Philips Electronics, N.V., headquartered in Eindhoven, the Netherlands. We have been authorized by both the assignee of record and NXP Semiconductors to convey herein that the entire right, title and interest of the instant patent application has been transferred to NXP Semiconductors.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-15 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

A minor grammatical amendment to claim 3, submitted in Response to Final Office Action paper dated November 22, 2006, was not entered by the Examiner. See Advisory Action dated December 18, 2006. No other amendments have been filed subsequent to the Final Office Action dated October 2, 2006.

V. Summary of Claimed Subject Matter

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a voltage controlled oscillator for generating a quadrature periodical output signal adjustable to frequencies in a relative wide range (*see, e.g.*, Fig. 1 and paragraph 0017). The voltage controlled oscillator includes a LC tank circuit (L, C, and R) coupled to a modulator means (2) for controlling an oscillation frequency of the LC tank circuit in response to a control signal V_T and coupled to an amplifier means (1) via an adder (3), the adder providing feedback to the LC tank circuit.

Commensurate with independent claim 7, an example embodiment of the present invention is directed to a method, for use with an LC-type tank circuit (L, C, and R) having an inductive current path (L) and a capacitive current path (C), for generating a quadrature periodical output signal (Vo) adjustable to frequencies in a relative wide range (*see, e.g.,* Fig. 2 and paragraph 0018). The method includes from a first high-impedance node (input to 20), generating a first buffered signal (output of 20) indicative of a level of current through the inductive path (L) of the LC-type tank circuit (L, C, and R) and from a second high-impedance node (input to 10), generating a second buffered signal (output of 10) indicative of a level of current through the capacitive path (C) of the LC-type tank circuit. The method further includes in response to a control signal V_T, quadrature modulating (21) the first buffered signal and producing a modulated signal (output of 21) therefrom, amplifying (11) the second buffered signal and producing an amplified signal (output of 11) therefrom, and adding the modulated signal and the amplified signal (node 3) and, in response thereto, providing a feedback signal (I) to the LC tank circuit (L, C, and R).

Commensurate with independent claim 11, an example embodiment of the present invention is directed to an arrangement, for use with an LC-type tank circuit (L, C, and R) having an inductive current path (L) and a capacitive current path (C), for generating a quadrature periodical output signal (Vo) adjustable to frequencies in a relative wide range (*see, e.g.,* Fig. 2 and paragraph 0018). The arrangement includes first high-impedance node (input to 20) means for generating a first buffered signal (output of 20) indicative of a level of current through the inductive path (L) of the LC-type tank circuit (L, C, and R) and second high-impedance node (input to 10) means for generating a second buffered signal (output of 10) indicative of a level of current through the capacitive path (C) of the LC-type tank circuit. The arrangement further includes means (21), responsive to a control signal (V_T), for quadrature modulating the first buffered signal (output of 20) and producing a modulated signal therefrom, means (11) for amplifying the second buffered signal and producing an amplified signal (output of 11) therefrom, and means (3) for adding the modulated signal (output of 21) and the amplified signal (output of 11) and, in response thereto, providing a feedback signal (I) to the LC tank circuit (L, C, and R).

Commensurate with independent claim 12, an example embodiment of the present invention is directed to an arrangement, for use with an LC-type tank circuit (L, C, and R) having an inductive current path (L) and a capacitive current path (C), for generating a quadrature periodical output signal (Vo) adjustable to frequencies in a relative wide range (*see, e.g.*, Fig. 2 and paragraph 0018). The arrangement includes a first high-impedance node circuit (20) to generate a first buffered signal (output of 20) indicative of a level of current through the inductive path (I) of the LC-type tank circuit (L, C, and R) and a second high-impedance node circuit (10) to generate a second buffered signal (output of 10) indicative of a level of current through the capacitive path (C) of the LC-type tank circuit. The arrangement further includes a quadrature modulator (21) to, in response to a control signal (V_T), quadrature modulate the first buffered signal (output of 20) and produce a modulated signal (output of 21) therefrom, an amplifier (11) to amplify the second buffered signal (output of 10), thereby producing an amplified signal (output of 11), and a circuit (3) to add the modulated signal and the amplified signal and, in response thereto, to provide a feedback signal (I) to the LC tank circuit (L, C, and R).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

1. Claims 1-5 stand rejected under 35 U.S.C. § 102(b) over Henrion (U.S. 6,198,360).

2. Claims 6-15 stand rejected under 35 U.S.C. § 103(a) over Henrion (U.S. 6,198,360) in view of Albon *et al.* (U.S. 6,683,509).

VII. Argument

A. The Section 102(b) rejection of claims 1-5 over Henrion.

1. Claims 1-5: The rejections are improper because the Examiner fails to present prior art that teaches the claimed invention as a whole.

The Section 102(b) rejection of claims 1-5 must be reversed because the cited portions of the Henrion reference do not correspond to all of the claimed limitations, including those directed to an adder that provides feedback to the LC tank circuit. Specifically, the asserted adder of the Henrion reference does not provide feedback to the LC tank circuit. Rather, in violation of M.P.E.P. § 2131, the Examiner has erroneously pieced together portions of different embodiments of the Henrion reference (*i.e.*, one embodiment contains a feedback signal while another contains the asserted adder) without showing how these portions work together to arrive at the claimed invention.

Appellant submits that the Examiner's citation purporting to support feedback (*i.e.*, Henrion, Col. 3, lines 40-45) discusses feedback relative to Figure 3 of Henrion, which has a configuration different from Figure 2, and as such, does not teach that the nodes asserted in the circuit of Figure 2 provide feedback to the LC tank circuit as the claimed limitations require. The Examiner has failed to show how the two pieces of these two distinct embodiments (figures 2 and 3) could be made to work together. Thus, Appellant submits that the Examiner's assertion that Figure 3 of the Henrion reference teaches feedback is irrelevant and insufficient to show that the asserted adder (of Figure 2) is taught to provide feedback of any kind. More specifically, the Examiner cites to various components of FIG. 2

of the Henrion reference, such as an asserted correspondence between transistors Q9, Q10 and the claimed the modulator means, to transistors Q1-Q4 and the claimed amplifier means, and nodes between R1 and L1 and between R2 and L2 and the claimed adder. Appellant notes that the relevant discussion of Figure 2 (*i.e.*, Henrion, Col. 3, lines 7-30) does not specifically mention these nodes, but does teach that MOS transistors M1-M4 operate as amplifiers for signals derived from inductors L1 and L2 summed with current from capacitors C1 and C2 in resistors R1 and R2. The Henrion reference, however, does not teach that the nodes provide feedback to the LC tank circuit as required by the claimed adder (*see, e.g.*, Henrion, Figure 2). Moreover, review of the Henrion reference reveals that, with regard to Figure 2, the feedback is taught to be provided through resistors R3 and R4 at nodes VOUTN and VOUTP, respectively (*see, e.g.*, Henrion, Col. 3, lines 1-6). In contrast, the Examiner's asserted nodes are taught to be used to provide an amplified signal from the LC circuit using MOS amplifiers M1-M4 (*see, e.g.*, Henrion, Col. 3 lines 6-30). Thus, while the Henrion reference teaches certain embodiments may implement feedback generally, the asserted adder nodes do not provide this feedback. According, the Henrion reference fails to teach correspondence to each limitation of the claimed invention.

In view of the above, the Henrion reference fails to provide teaching or suggestion of each claimed limitation; Appellant therefore submits that the Section 102(b) rejection of claims 1-5 is improper and must be reversed.

B. The Section 103(a) rejection of claims 6-15 over Henrion in view of Albon.

1. Claim 6: The Section 103(a) rejection is improper because the Examiner fails to present prior art that teaches the claimed invention as a whole and because the Examiner fails to provide motivation to modify Henrion with the teachings of Albon.

The Examiner fails to present prior art that teaches the claimed invention as a whole:

The Section 103(a) rejection of claim 6, which depends from claim 1, must be reversed in view of the above discussion regarding the rejection of independent claim 1. That is, where an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *See, e.g., In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

The Examiner fails to provide motivation to modify Henrion with the teachings of Albon:

The Section 103(a) rejection of claim 6 must be reversed because the Examiner fails to provide adequate motivation to modify the Henrion reference using the teachings of the Albon reference. The Examiner admits that the Henrion reference does not disclose any PLL implementation for a TV tuner application and then asserts that the combination of the differential oscillator of the Henrion reference is conventional because the Albon reference (rather than Applicant's invention with the claimed feedback) generally uses some type of a VCO and a PLL. Accordingly, the Examiner has provided an unsupported, personal opinion that the Henrion circuit is conventional to TV tuning circuits. Pursuant to M.P.E.P. § 2144.03, Appellant should have been presented with the explicit basis on which the examiner bases the personal opinion and been allowed to challenge the assertion in the next reply after the Office action. Rather than addressing the specific Henrion circuit relied upon, the Examiner merely reiterated that the Albion reference (generally) taught differential oscillators and PLLs are used in TV tuning circuits. To the extent that the Examiner appears to be taking official notice that the combination of the specific VCO of the Henrion reference with the circuit of the Albon reference is conventional, Appellant asserts that pursuant to M.P.E.P. § 2144.03(A), it is not appropriate for the Examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known. Moreover, where assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art, the assertions must always be supported by citation to some reference work recognized as standard in the pertinent art. (M.P.E.P. § 2144.03(A), citing *In re Ahlert*, 424 F.2d at 1091, 165 USPQ at 420-21). Thus, the Examiner's assertion that the specific circuit shown by Figure 2 of the Henrion reference is conventionally used by TV tuning circuits, without further support, is improper. Specifically, Appellant submits that the Examiner lacks support for the assertion that "these VCO oscillators are implemented conventionally with TV tuning circuits" (*see, e.g.*, the Final Office Action dated October 2, 2006, page 3, line 21). Appellant submits that there are a variety of VCOs, not all of which would be suitable for use with the circuit taught by the Albon reference (*e.g.*, Figure 1), and that the Albon VCO bears

little resemblance to the circuit taught by Figure 2 of the Henrion reference. Thus, the cited portions of the references do not support the Examiner's assertion that the Figure 2 circuit of the Henrion reference is a conventional VCO used by TV tuners. Appellant submits that without further support, the assertion is improper and the Section 103(a) rejection of claim 6 is improper and must be reversed.

2. **Claims 7-15: The Section 103(a) rejections of claims 7-15 over Henrion in view of Albon is improper because the Examiner fails to present prior art that teaches the claimed invention as a whole and because the Examiner fails to provide motivation to modify Henrion with the teachings Albon.**

The Examiner fails to present prior art that teaches the claimed invention as a whole:

The Section 103(a) rejections of claims 7-15 must be reversed because the cited portions of the Henrion and the Albon references do not correspond to all of the claimed limitations, including those directed to high-impedance nodes generating buffered signals indicative of the capacitive and inductive current levels of the LC tank circuit. Moreover, the cited references do not teach adding the modulated signal and the amplified signal to provide a feedback signal to the LC tank circuit, as discussed relative to the aforementioned impropriety of the Section 102(b) rejections based upon the Henrion reference.

The Section 103(a) rejections further must be reversed because the Examiner has asserted correspondence to the wrong claims, and thus, fails to present a *prima facie* case of obviousness. "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." *See* M.P.E.P. § 2143.03. The Examiner fails to even mention numerous claimed limitations and instead asserts correspondence to the wrong claims while citing to portions of the Henrion reference that do not teach correspondence to the claimed limitations. For instance, the Examiner asserts that transistors Q1-Q4 correspond to an "amplifier buffer means," and such a limitation is not present in the instance claims. (See also, asserted correspondence to a modulator having a Gilbert cell configuration and a modulator means). Accordingly, Examiner has failed to address the claimed limitations and instead erroneously addresses limitations not present in the instance claims. Moreover, upon a review of the asserted references, Appellant is unable

to discern how the cited transistors correspond to each of the claimed limitations. For example, the Examiner fails to address claimed limitations directed to a first high-impedance node that generates a first buffered signal from the inductive path and a second high impedance node that generates a second buffered signal from the capacitive path.

The Examiner has also asserted that high impedance is inherently present in the teachings of the Henrion reference. Appellant submits that the Examiner's assertion of inherency is improper and unsupported by the Henrion reference. "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art" (*see, e.g.*, M.P.E.P § 2112(IV)). The Examiner merely states that "(w)ith regards the high impedance, this is inherent due to the fact that the oscillator output has to be isolated from loading effects that may affect the frequency when coupled to other elements;" however, the Examiner fails to provide support for this statement from the references or otherwise. Moreover, assertions as to whether it would be possible for high impedance nodes to be attached to outputs VOUTN and VOUTP is entirely irrelevant because the Examiner has not even asserted that the VOUTN and VOUTP nodes would otherwise correspond to the claimed limitations including the limitations directed to the relationship between different high impedance nodes. Instead, the erroneously asserted high impedance nodes are discussed independent of (without explanation relative to) the remainder of the Examiner's asserted correspondence.

More specifically, Appellant notes that the Examiner's asserted correspondence shows that the alleged, corresponding nodes are not high impedance (*see, e.g.*, Henrion, Figure 2). Thus, the Examiner's assertion of inherency is also irrelevant because the asserted combination does not have the claimed high impedance nodes, which generate buffered signals for the capacitive and inductive paths as required by the claimed limitations. More specifically, Figure 2 of the Henrion reference shows that signals from the inductive path are amplified through MOS devices M1-M4. Appellant submits that when such MOS devices are active, they have almost no impedance from source to drain. Accordingly, when the MOS devices operate to generate a corresponding signal, the asserted nodes would see

almost no impedance. Accordingly, the cited references fail to teach each of the claimed limitations.

Appellant further notes that the Examiner's asserted adder does not add the modulated signal and the amplified signal as required by the claimed limitations (*see, e.g.*, Henrion, Col 3, lines 10-20). Appellant submits that the asserted adder does not even receive an amplified signal from the Examiner's amplifier buffer means, and thus, cannot function to add such an amplified signal.

Moreover, the Section 103(a) rejection of claims 7-15 must be reversed because the Examiner fails show correspondence to the claimed limitations directed to an adder that provides feedback to the LC tank circuit, for the same reasons discussed above regarding claims 1-5.

In view of the above, the Henrion reference fails to provide teaching or suggestion of each claimed limitation; Appellant therefore submits that the Section 103(a) rejection of claims 7-15 is improper and must be reversed.

The Examiner fails to provide motivation to modify Henrion with the teachings of Albon:

The Section 103(a) rejection of claims 7-15 must be reversed because the Examiner fails to provide adequate motivation or suggestion to modify the Henrion reference using the teachings of the Albon reference for the same reasons discussed above regarding claim 6. Therefore, the rejections of claims 7-15 are also improper and must be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-15 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/527,946)

1. (*Previously presented*) For generating a quadrature periodical output signal adjustable to frequencies in a relative wide range, a voltage controlled oscillator comprising a LC tank circuit coupled to a modulator means for controlling an oscillation frequency of the LC tank circuit in response to a control signal and coupled to an amplifier means via an adder, the adder providing feedback to the LC tank circuit.

2. (*Previously presented*) An oscillator as claimed in claim 1, wherein the modulator means comprises a series coupling of a buffer and a modulator.

3. (*Previously presented*) An oscillator as claimed in claim 1, wherein the amplifier means comprise a series coupling of an another buffer and an amplifier.

4. (*Previously presented*) An oscillator as claimed in claim 3, wherein the amplifier is a transconductance amplifier.

5. (*Previously presented*) An oscillator as claimed in claim 1, wherein the amplifier means is a transconductance amplifier , the modulator means is a Gilbert cell modulator and the adder is a node.

6. (*Previously presented*) A phase locked loop comprising an oscillator as claimed in claim 1 for use in a large tuning TV tuner.

7. (*Previously presented*) For use with an LC-type tank circuit having an inductive current path and a capacitive current path, a method for generating a quadrature periodical output signal adjustable to frequencies in a relative wide range, the method comprising:

from a first high-impedance node, generating a first buffered signal indicative of a level of current through the inductive path of the LC-type tank circuit;

from a second high-impedance node, generating a second buffered signal indicative of a level of current through the capacitive path of the LC-type tank circuit;

in response to a control signal, quadrature modulating the first buffered signal and producing a modulated signal therefrom;

amplifying the second buffered signal and producing an amplified signal therefrom; and

adding the modulated signal and the amplified signal and, in response thereto, providing a feedback signal to the LC tank circuit.

8. (*Previously presented*) The method of claim 7, wherein the step of amplifying uses a transconductance amplifier.

9. (*Previously presented*) The method of claim 7, further including the step of using a phase-locked-loop circuit to control the periodic output signal.

10. (*Previously presented*) The method of claim 9, wherein the periodic output signal is used in a TV tuner.

11. (*Previously presented*) For use with an LC-type tank circuit having an inductive current path and a capacitive current path, an arrangement for generating a quadrature periodical output signal adjustable to frequencies in a relative wide range, the arrangement comprising:

first high-impedance node means for generating a first buffered signal indicative of a level of current through the inductive path of the LC-type tank circuit;

second high-impedance node means for generating a second buffered signal indicative of a level of current through the capacitive path of the LC-type tank circuit;

means, responsive to a control signal, for quadrature modulating the first buffered signal and producing a modulated signal therefrom;

means for amplifying the second buffered signal and producing an amplified signal therefrom; and

means for adding the modulated signal and the amplified signal and, in response thereto, providing a feedback signal to the LC tank circuit.

12. (*Previously presented*) For use with an LC-type tank circuit having an inductive current path and a capacitive current path, an arrangement for generating a quadrature periodical output signal adjustable to frequencies in a relative wide range, the arrangement comprising:

first high-impedance node circuit to generate a first buffered signal indicative of a level of current through the inductive path of the LC-type tank circuit;

second high-impedance node circuit to generate a second buffered signal indicative of a level of current through the capacitive path of the LC-type tank circuit;

a quadrature modulator to, in response to a control signal, quadrature modulate the first buffered signal and produce a modulated signal therefrom;

an amplifier to amplify the second buffered signal, thereby producing an amplified signal; and

a circuit to add the modulated signal and the amplified signal and, in response thereto, and to provide a feedback signal to the LC tank circuit.

13. (*Previously presented*) The arrangement of claim 12, wherein the amplifier is a transconductance amplifier.

14. (*Previously presented*) The arrangement of claim 12, further including a phase-locked-loop circuit to control the periodic output signal.

15. (*Previously presented*) The arrangement of claim 14, further including a TV tuner to facilitate tuning.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.